

REMARKS

The applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Status of the Claims

Claims 1, 2, 4, 7-12, 14, 15, 17 and 19-21 are pending in the application. Claims 1, 12 and 21 are independent. The amendments to claims 1 and 12 also find support at page 12, lines 16-18 (paragraph 0050) of the specification.

Withdrawal of Claim 21

At page 2 of the Office Action, the Examiner asserts that claim 21 is being withdrawn as not being directed to the originally presented invention.

However, an election restriction requirement was issued on December 3, 2003, which restricted the invention into two groups:

- I. Claims 1-11, drawn to a liquid crystal display; and
- II. Claims 12-20 drawn to a method of fabricating a liquid crystal display.

On January 5, 2004, a Response was filed that traversed the restriction requirement and presented remarks noting that the Examiner has previously

performed consideration and search, and that no undue burden was placed upon the Examiner to examine all the claims of the invention.

On April 13, 2005, the Examiner issued an Office Action that *inter alia* withdrew the restriction requirement.

As a result, this is no restriction requirement in the instant application that the Examiner can utilize as a basis to withdraw claim 21.

Further, even if one assumes *arguendo* that the restriction requirement has not been withdrawn, it is respectfully noted that the Response of January 5, 2004 elected group I, drawn to a liquid crystal display, and claim 21 is also drawn to a liquid crystal display. As a result, claim 21 is clearly drawn to an elected invention.

The examination of claim 21 on the merits is accordingly respectfully requested.

Rejections Based Upon Rho

Claims 1, 2, 7, 8, 10-12, 17 and 19-20 are rejected under 35 U.S.C. §103(a) as being obvious over Rho (U.S. Patent 6,057,896) in view of Kan (JP 09-232580), Jeong (U.S. Patent 6,137,551) and Kim (U.S. Patent 5,731,856). The Examiner adds the teachings of Shimada (U.S. Patent 6,424,399) to the aforesaid rejection to reject claims 4, 9, 14 and 15. Applicant respectfully traverses.

The Present Invention And Its Advantages

The present invention pertains to a liquid crystal display having a novel geometry that increases aperture ratio and also increases the capacitance of the storage capacitor. The streamlined geometry of the inventive display permits connection of the pixel electrode to the drain by using a protective layer covering the source electrode, the drain electrode and some portions of the pixel electrode. That is, the pixel electrode can connect to the drain without recourse to a contact hole.

One of the many important aspects of the invention also lies in a buffer metal layer being formed on the source and drain electrodes (Claims 1 and 12). This buffer metal layer reduces contact resistance (claims 9 and 14).

The invention has many embodiments, and a typical embodiment is in instant product claim 1:

1. A liquid crystal display, comprising:
 - a gate electrode over a substrate;
 - a gate insulating film entirely deposited over the substrate to cover said gate electrode;
 - an active layer formed on said gate insulating film which overlaps with said gate electrode;
 - an ohmic contact layer formed on said active layer;
 - a source electrode formed on said ohmic contact layer;
 - a drain electrode formed on said ohmic contact layer, the drain electrode being opposed to said source electrode to form a channel;
 - a buffer layer formed over said source and drain electrodes;

a storage electrode formed at a pixel cell area of a same layer as said gate electrode, said storage electrode comprising a transparent conductive material;

an auxiliary storage electrode connected to said storage electrode;

a pixel electrode formed to oppose to said storage electrode having said gate insulating film in between said pixel electrode and said storage electrode, and said pixel electrode being electrically connected with said drain electrode without using a contact hole; and

a protective layer covering said source electrode, said drain electrode and some portions of the pixel electrode.

Another preferred embodiment of the invention is set forth in method claim 12:

12. A method of fabricating a liquid crystal display, comprising:
 - forming a gate electrode and a gate line over a substrate and at the same time forming a storage electrode in a same layer where said gate electrode and said gate line are formed, said storage electrode being formed of a transparent conductive material;
 - forming an auxiliary storage electrode connecting to said storage electrode;
 - forming a gate insulating film to cover said gate electrode, said gate line and said storage electrode;
 - forming an active layer over said gate insulating film to overlap with said gate electrode;
 - forming an ohmic contact layer over said active layer;
 - forming a source electrode and a drain electrode by patterning to expose said active layer;
 - forming a buffer metal layer over said source electrode and said drain electrode;
 - forming a pixel electrode opposed to said storage electrode having said gate insulating film in between said pixel electrode and said storage electrode, and said pixel electrode being contacted with said drain electrode without using a contact hole;
 - forming a protective layer over said source electrode and said drain electrode;
 - forming a contact hole that pierces said protective layer; and

forming a data line crossed with said gate line and connected with said source electrode through said contact hole.

Distinctions Of The Invention Over Rho And The Secondary References

Rho pertains to liquid crystal displays using an organic insulating material for a passivation layer and/or a gate insulating layer. The Examiner turns to Figure 3 of Rho, which is reproduced below:

FIG.3

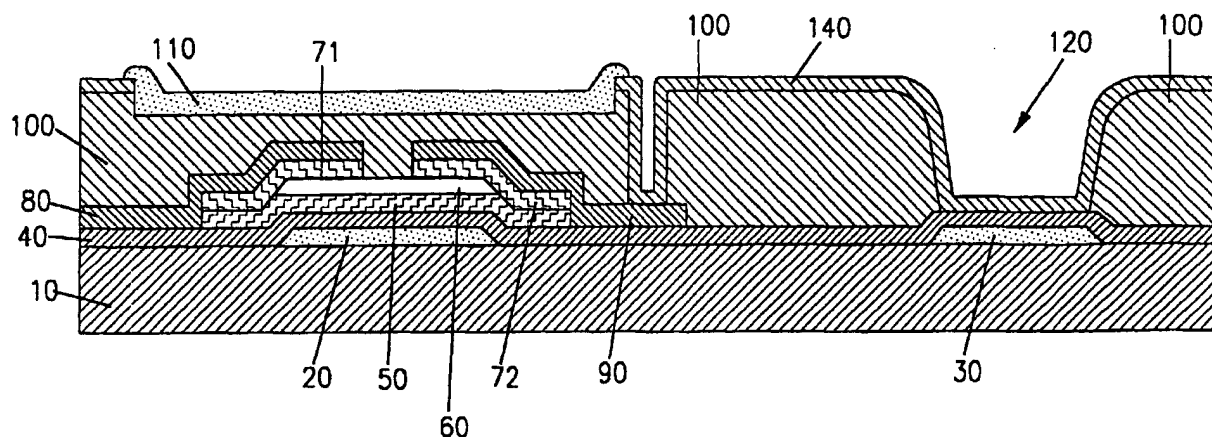


Figure 3 of Rho shows a gate insulating layer **40** on a gate electrode **20**. A TFT structure (source electrode **80**, drain electrode **90**, amorphous silicon layer **50**, etch stopper layer **60**, and ohmic contact layer **71**, **72**) is formed over the gate insulating layer **40**. Figure 3 of Rho also shows a storage capacitor

electrode **30** and a pixel electrode **140**. A notable feature of Rho's technology is the passivation layer **100**, which necessitates the utilization of a contact hole.

Rho fails to disclose or suggest a technology where the pixel electrode can connect to the drain electrode without recourse to a contact hole.

Rho at column 5, lines 7-8 states: "The passivation layer **100** has a contact hole **130** exposing the drain electrode **90**. . ." In contrast, the invention has "said pixel electrode being electrically connected with said drain electrode without using a contact hole." See claims 1 and 12.

Rho also teaches away from the invention. Rho at column 5, lines 41-47 states:

The storage capacitor electrode **30** and the pixel electrode **140** form a storage capacitor. Because there is thick passivation layer **100** between the two electrodes **30** and **140**, the storage capacitance may not be sufficiently large. To compensate for the storage capacitance, the portion of the passivation layer between the two electrodes **30** and **140** may be removed or become thinned.

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). A *prima facie* case of

obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

In contrast, one typical object of the present invention is to increase storage capacity, and this is accomplished by eliminating the thick passivation layer so that the pixel electrode can contact the drain electrode directly, and not through a contact hole. In part, the reduction of contact resistance by the buffer metal layer permits this electrode geometry.

In contrast, Rho merely teaches thinning the passivation layer, and one having ordinary skill would not be motivated by this teaching to have the pixel electrode contact the drain electrode directly, and not through a contact hole.

Rho additionally provides no motivation to one having ordinary skill in the art to produce a high aperture ratio liquid crystal display having high capacitance where the pixel electrode can contact the drain electrode directly, and not through a contact hole.

Also, the Examiner unequivocally admits to the failures of Rho. At page 4, lines 12-13 of the Office Action, the Examiner states: "Rho does not appear to explicitly specify a buffer layer formed over said source and drain electrodes." (Emphasis in original). At page 4, lines 19-20 of the Office Action, the Examiner states: "Rho does not appear to explicitly specify said storage

electrode comprising a transparent conductive material and an auxiliary storage electrode connected to said storage electrode." (Emphasis in original). At page 5, lines 14-15 of the Office Action, the Examiner states: "Rho does not appear to explicitly specify a protective layer covering said source electrode and some portions of the pixel electrode." At page 7, lines 11-12 of the Office Action, the Examiner states: "Rho does not appear to explicitly specify that the source and drain electrodes further comprises a buffer layer of molybdenum, titanium or tantalum."

The Examiner turns to the secondary references to supply the deficiencies of Rho. The Examiner turns to Kan for teachings about buffer layers. The Examiner turns to Jeong for teachings pertaining to a transparent pixel electrode (of e.g. ITO) and a storage electrode. The Examiner turns to Kim for teachings pertaining to a protective layer. The Examiner turns to Shimada for teachings pertaining to a buffer layer of molybdenum, titanium or tantalum.

However, these teachings of Kan, Jeong, Kim and Shimada fail to address the fundamental inability of Rho to suggest the present invention. That is, the failure of Rho to suggest a high aperture ratio liquid crystal display having high capacitance where the pixel electrode can contact the drain electrode directly, and not through a contact hole.

Also, the Examiner rejects the claims of the present invention by using five references: Rho, Kan, Jeong, Kim and Shimada.

However, this complicated utilization of the prior art can only be obtained through the application of impermissible hindsight reconstruction.

“Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is a rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.” *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (CAFC 1999). *See also In re Kotzab*, 217 F.3d 1365, 1369-70, 55 USPQ2d 1313, 1316 (CAFC 2000). “Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor’s disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight.” *Dembiczak* at 50 USPQ2d 1617. “The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time.” *Dembiczak* at 50 USPQ2d 1617. “The patent examination process centers on prior art and the examination thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness . . . The factual inquiry must be thorough and searching. It must be based on objective evidence of

record.” *In re Lee*, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-44 (Fed. Cir. 2002).

In this case, the cited art references are conventional art in which the pixel is formed on the protective layer covering the drain electrode and connected with the drain electrode through a contact hole formed by patterning the protective layer. However, in the invention, the pixel electrode is formed over the drain electrode and patterned. Afterwards, the protective layer is covered and patterned to open many portions of the pixel electrode with some portions overlapping the drain electrode. That is, the pixel area portion of the pixel electrode is opened and some portions of the pixel electrode are covered by the protective layer.

The primary reference of Rho fails to disclose or suggest a technology where the pixel electrode can connect to the drain electrode without recourse to a contact hole. Rho additionally teaches away from the invention. The secondary references fail to address the deficiencies of Rho.

However, none of the secondary references addresses the failure of Rho to teach or suggest a liquid crystal display having a pixel electrode that can contact the drain electrode directly and not through a contact hole (claims 1 and 12).

As a result, one having ordinary skill in the art would not be motivated by Rho and the secondary references to produce to invention of claims 1 and

12. A *prima facie* case of obviousness has thus not been made. Even if the references could be combined, a *prima facie* case of obviousness has still not been made over independent claims 1 and 12 because *inter alia* the primary reference of Rho teaches away from the invention and impermissible hindsight reconstruction. Claims depending upon independent claims 1 and 12 are patentable for at least the above reasons.

These rejections are overcome and withdrawal thereof is respectfully requested.

Prior Art

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supercedes. Additional remarks are accordingly not necessary.

Foreign Priority

The Examiner has acknowledged foreign priority most recently in the Office Action of November 1, 2005.

Drawings

The Examiner has accepted the drawing figures in the Office Action of November 1, 2005.

Conclusion

The Examiner's rejections have been overcome, obviated or rendered moot. No issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner, Ph.D. (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Application No.: 10/028,687
Amendment filed February 1, 2006
Response to Office Action of November 1, 2005

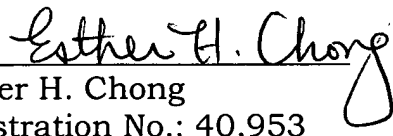
Docket No.: 2658-0276P

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: February 1, 2006



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